

What is claimed is:

1.           A spread-spectrum demodulator comprising:
  - 2               a spreading code generating section which
  - 3 generates a spreading code for correlating with a
  - 4 received spread signal;
  - 5               a correlation value computing section which
  - 6 computes a correlation value between the spread signal
  - 7 and the spreading code output from said spreading code
  - 8 generating section;
  - 9               a data signal demodulating section which
  - 10 detects a peak of an output from said correlation value
  - 11 computing section and demodulates a data signal on the
  - 12 basis of the detected peak;
  - 13               a peak signal detecting section which detects
  - 14 the peak of the output from said correlation value
  - 15 computing section; and
  - 16               a spreading code generation control section
  - 17 which changes a shifting direction of the spreading code
  - 18 relative to the spread signal every time a peak is
  - 19 detected by said peak signal detecting section.
  
2.           A spread-spectrum demodulator comprising:
  - 2               N (N is an integer not less than 2)
  - 3 sample/hold circuits each of which samples/holds a
  - 4 received spread signal;
  - 5               a sample/hold control circuit which receives a

6 first clock having the same frequency as that of a clock  
7 used to spread the baseband signal, and performs control  
8 to make said N sample/hold circuits sequentially perform  
9 sample/hold operation in synchronism with the first  
10 clock;  
11           a first spreading code generating circuit  
12 which generates N first spreading codes in synchronism  
13 with a second clock;  
14           a second spreading code generating circuit  
15 which generates N second spreading codes obtained by  
16 rearranging the first spreading codes in reverse order  
17 in synchronism with the second clock;  
18           N multipliers which multiply signals output  
19 from said sample/hold circuits and spreading codes  
20 output from said first spreading code generating circuit  
21 or said second spreading code generating circuit for  
22 each corresponding signal;  
23           an adder which adds outputs from said N  
24 multipliers;  
25           a peak detector which detects a peak of an  
26 output from said adder and demodulates a data signal on  
27 the basis of the detected peak; and  
28           a spreading code control circuit which  
29 alternately switches inputting of the first spreading  
30 codes from said first spreading code generating circuit  
31 to said multipliers and inputting of the second  
32 spreading codes from said second spreading code

33 generating circuit to said multipliers every time the  
34 peak is detected by said peak detector.

3.           A demodulator according to claim 2, wherein  
2           said first spreading code generating circuit  
3 comprises N flip-flop circuits of a first flip-flop  
4 circuit group each of which shifts the first spreading  
5 code in synchronism with the second clock, a first  
6 exclusive-OR circuit which receives outputs from a  
7 plurality of flip-flop circuits of said first flip-flop  
8 circuit group, and a first switch group which openably  
9 cascades the flip-flop circuits of said first flip-flop  
10 circuit group and openably connects an output of said  
11 first exclusive-OR circuit to an input of a first-stage  
12 flip-flop circuit in said first flip-flop circuit group,  
13           said second spreading code generating circuit  
14 comprises N flip-flop circuits of a second flip-flop  
15 circuit group each of which shifts the second spreading  
16 code in a reverse direction relative to the first  
17 spreading code in synchronism with the second clock, a  
18 second exclusive-OR circuit which receives outputs from  
19 a plurality of flip-flop circuits in said second  
20 flip-flop circuit group, and a second switch group which  
21 openably cascades the flip-flop circuits of said second  
22 flip-flop circuit group and openably connects an output  
23 of said second exclusive-OR circuit to an input of a  
24 first-stage flip-flop circuit in said second flip-flop

25 circuit group, and  
26               said spreading code control circuit which  
27 alternately switches control operation of turning on  
28 said first switch group and control operation of turning  
29 on said second switch group every time the peak is  
30 detected by said peak detector.

4.           A spread-spectrum demodulator comprising:  
2            N (N is an integer not less than 2)  
3 sample/hold circuits each of which samples/holds a  
4 received spread signal in synchronism with a first clock  
5 having the same frequency as that of a clock used to  
6 spread the baseband signal;  
7            a spreading code generating circuit which  
8 generates N spreading codes in synchronism with a second  
9 clock;  
10           N multipliers which multiply signals output  
11 from said sample/hold circuits and spreading codes  
12 output from said spreading code generating circuit for  
13 each corresponding signal;  
14           an adder which adds outputs from said N  
15 multipliers;  
16           a peak detector which detects a peak of an  
17 output from said adder and demodulates a data signal on  
18 the basis of the detected peak; and  
19           a clock control circuit which controls  
20 inputting of the second clock to said spreading code

21 generating circuit in accordance with detection of the  
22 peak by said peak detector.

5. A demodulator according to claim 4, wherein  
2 said clock control circuit alternately switches stoppage  
3 and resumption of inputting of the second clock to said  
4 spreading code generating circuit every time the peak is  
5 detected by said peak detector.

6. A demodulator according to claim 4, wherein  
2 said clock control circuit stops inputting the second  
3 clock to said spreading code generating circuit for a  
4 predetermined period of time when the peak is detected  
5 by said peak detector.

7. A spread-spectrum demodulator comprising:  
2 a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;  
6 (N - 1) (N is an integer not less than 2)  
7 register circuits which output (N - 1) signals by  
8 delaying an output signal from said comparator circuit  
9 by one period to (N - 1) periods of the first clock,  
10 respectively;  
11 a spreading code generating circuit which  
12 generates N spreading codes in synchronism with a second

13 clock;  
14               N multipliers which multiply signals output  
15 from said comparator circuit and said register circuits  
16 and spreading codes output from said spreading code  
17 generating circuit for each corresponding signal;  
18               an adder which adds outputs from said N  
19 multipliers;  
20               a peak detector which detects a peak of an  
21 output from said adder and demodulates a data signal on  
22 the basis of the detected peak; and  
23               a clock control circuit which controls  
24 inputting of the second clock to said spreading code  
25 generating circuit in accordance with detection of the  
26 peak by said peak detector.

8.           A demodulator according to claim 7, wherein  
2 said clock control circuit alternately switches stoppage  
3 and resumption of inputting of the second clock to said  
4 spreading code generating circuit every time the peak is  
5 detected by said peak detector.

9.           A demodulator according to claim 7, wherein  
2 said clock control circuit stops inputting the second  
3 clock to said spreading code generating circuit for a  
4 predetermined period of time when the peak is detected  
5 by said peak detector.

10.           A spread-spectrum demodulator comprising:

2               a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;

6               (N - 1) (N is an integer not less than 2)  
7 register circuits which output (N - 1) signals by  
8 delaying an output signal from said comparator circuit  
9 by one period to (N - 1) periods of the first clock,  
10 respectively;

11              a first spreading code generating circuit  
12 which generates N first spreading codes in synchronism  
13 with a second clock;

14              a second spreading code generating circuit  
15 which generates N second spreading codes obtained by  
16 rearranging the first spreading codes in reverse order  
17 in synchronism with the second clock;

18              N multipliers which multiply signals output  
19 from said comparator circuit and said register circuits  
20 and spreading codes output from said first spreading  
21 code generating circuit or said second spreading code  
22 generating circuit for each corresponding signal;

23              an adder which adds outputs from said N  
24 multipliers;

25              a peak detector which detects a peak of an  
26 output from said adder and demodulates a data signal on  
27 the basis of the detected peak; and

28                   a spreading code control circuit which  
29 alternately switches inputting of the first spreading  
30 codes from said first spreading code generating circuit  
31 to said multipliers and inputting of the second  
32 spreading codes from said second spreading code  
33 generating circuit to said multipliers every time the  
34 peak is detected by said peak detector.

11.               A demodulator according to claim 10, wherein  
2                   said register circuit comprises a flip-flop  
3 circuit,  
4                   said first spreading code generating circuit  
5 comprises N flip-flop circuits of a first flip-flop  
6 circuit group each of which shifts the first spreading  
7 code in synchronism with the second clock, a first  
8 exclusive-OR circuit which receives outputs from a  
9 plurality of flip-flop circuits of said first flip-flop  
10 circuit group, and a first switch group which openably  
11 cascades the flip-flop circuits of said first flip-flop  
12 circuit group and openably connects an output of said  
13 first exclusive-OR circuit to an input of a first-stage  
14 flip-flop circuit in said first flip-flop circuit group,  
15                   said second spreading code generating circuit  
16 comprises N flip-flop circuits of a second flip-flop  
17 circuit group each of which shifts the second spreading  
18 code in a reverse direction relative to the first  
19 spreading code in synchronism with the second clock, a



20 second exclusive-OR circuit which receives outputs from  
21 a plurality of flip-flop circuits in said second  
22 flip-flop circuit group, and a second switch group which  
23 openably cascades the flip-flop circuits of said second  
24 flip-flop circuit group and openably connects an output  
25 of said second exclusive-OR circuit to an input of a  
26 first-stage flip-flop circuit in said second flip-flop  
27 circuit group, and  
28               said spreading code control circuit which  
29 alternately switches control operation of turning on  
30 said first switch group and control operation of turning  
31 on said second switch group every time the peak is  
32 detected by said peak detector.

12.           A spread-spectrum demodulator comprising:  
2               N (N is an integer not less than 2)  
3 sample/hold circuits each of which samples/holds a  
4 received spread signal;  
5               a sample/hold control circuit which receives a  
6 first clock having the same frequency as that of a clock  
7 used to spread the baseband signal, and performs control  
8 to make said N sample/hold circuits sequentially perform  
9 sample/hold operation in synchronism with the first  
10 clock;  
11              a first spreading code generating circuit  
12 which generates N first spreading codes in synchronism  
13 with a second clock;

14               a second spreading code generating circuit  
15 which generates N second spreading codes obtained by  
16 rearranging the first spreading codes in reverse order  
17 in synchronism with the second clock;  
18               a polarity conversion circuit which outputs  
19 nearly half of the N spreading codes output from said  
20 first spreading code generating circuit or said second  
21 spreading code generating circuit which correspond to  
22 either newer or older spread signals in a reception  
23 order upon performing polarity conversion such that each  
24 of the spreading codes exhibits two polarity states,  
25 i.e., inverted and noninverted states, during one period  
26 of the second clock, and outputs remaining nearly half  
27 of the codes without any change,  
28               N multipliers which multiply signals output  
29 from said sample/hold circuits and spreading codes  
30 output from said polarity conversion circuit for each  
31 corresponding signal;  
32               an adder which adds outputs from said N  
33 multipliers;  
34               a peak detector which detects a peak of an  
35 output from said adder and demodulates a data signal on  
36 the basis of the detected peak; and  
37               a spreading code control circuit which  
38 alternately switches inputting of the first spreading  
39 codes from said first spreading code generating circuit  
40 to said polarity conversion circuit and inputting of the

41 second spreading codes from said second spreading code  
42 generating circuit to said polarity conversion circuit  
43 every time the peak is detected by said peak detector.

13. A demodulator according to claim 12, wherein  
2 said first spreading code generating circuit  
3 comprises N flip-flop circuits of a first flip-flop  
4 circuit group each of which shifts the first spreading  
5 code in synchronism with the second clock, a first  
6 exclusive-OR circuit which receives outputs from a  
7 plurality of flip-flop circuits of said first flip-flop  
8 circuit group, and a first switch group which openably  
9 cascades the flip-flop circuits of said first flip-flop  
10 circuit group and openably connects an output of said  
11 first exclusive-OR circuit to an input of a first-stage  
12 flip-flop circuit in said first flip-flop circuit group,  
13 said second spreading code generating circuit  
14 comprises N flip-flop circuits of a second flip-flop  
15 circuit group each of which shifts the second spreading  
16 code in a reverse direction relative to the first  
17 spreading code in synchronism with the second clock, a  
18 second exclusive-OR circuit which receives outputs from  
19 a plurality of flip-flop circuits in said second  
20 flip-flop circuit group, and a second switch group which  
21 openably cascades the flip-flop circuits of said second  
22 flip-flop circuit group and openably connects an output  
23 of said second exclusive-OR circuit to an input of a

24 first-stage flip-flop circuit in said second flip-flop  
25 circuit group, and  
26               said spreading code control circuit which  
27 alternately switches control operation of turning on  
28 said first switch group and control operation of turning  
29 on said second switch group every time the peak is  
30 detected by said peak detector.

14.           A spread-spectrum demodulator comprising:  
2               N (N is an integer not less than 2)  
3 sample/hold circuits each of which samples/holds a  
4 received spread signal;  
5               a sample/hold control circuit which receives a  
6 first clock having the same frequency as that of a clock  
7 used to spread the baseband signal, and performs control  
8 to make said N sample/hold circuits sequentially perform  
9 sample/hold operation in synchronism with the first  
10 clock;  
11              a first spreading code generating circuit  
12 which generates N first spreading codes in synchronism  
13 with a second clock;  
14              a second spreading code generating circuit  
15 which generates N second spreading codes obtained by  
16 rearranging the first spreading codes in reverse order  
17 in synchronism with the second clock;  
18              N multipliers which multiply signals output  
19 from said sample/hold circuits and spreading codes

20 output from said first spreading code generating circuit  
21 or said second spreading code generating circuit;  
22 a polarity conversion circuit which outputs  
23 nearly half of multiplier output signals from said N  
24 multipliers which correspond to either newer or older  
25 spread signals in a reception order upon performing  
26 polarity conversion such that each of the multiplier  
27 output signals exhibits two polarity states, i.e.,  
28 inverted and noninverted states, during one period of  
29 the second clock, and outputs remaining nearly half of  
30 the multiplier output signals without any change,  
31 an adder which adds outputs from said polarity  
32 conversion circuit;  
33 a peak detector which detects a peak of an  
34 output from said adder and demodulates a data signal on  
35 the basis of the detected peak; and  
36 a spreading code control circuit which  
37 alternately switches inputting of the first spreading  
38 codes from said first spreading code generating circuit  
39 to said multipliers and inputting of the second  
40 spreading codes from said second spreading code  
41 generating circuit to said multipliers every time the  
42 peak is detected by said peak detector.

15. A demodulator according to claim 14, wherein  
2 said first spreading code generating circuit  
3 comprises N flip-flop circuits of a first flip-flop

4 circuit group each of which shifts the first spreading  
5 code in synchronism with the second clock, a first  
6 exclusive-OR circuit which receives outputs from a  
7 plurality of flip-flop circuits of said first flip-flop  
8 circuit group, and a first switch group which openably  
9 cascades the flip-flop circuits of said first flip-flop  
10 circuit group and openably connects an output of said  
11 first exclusive-OR circuit to an input of a first-stage  
12 flip-flop circuit in said first flip-flop circuit group,  
13               said second spreading code generating circuit  
14 comprises N flip-flop circuits of a second flip-flop  
15 circuit group each of which shifts the second spreading  
16 code in a reverse direction relative to the first  
17 spreading code in synchronism with the second clock, a  
18 second exclusive-OR circuit which receives outputs from  
19 a plurality of flip-flop circuits in said second  
20 flip-flop circuit group, and a second switch group which  
21 openably cascades the flip-flop circuits of said second  
22 flip-flop circuit group and openably connects an output  
23 of said second exclusive-OR circuit to an input of a  
24 first-stage flip-flop circuit in said second flip-flop  
25 circuit group, and  
26               said spreading code control circuit which  
27 alternately switches control operation of turning on  
28 said first switch group and control operation of turning  
29 on said second switch group every time the peak is  
30 detected by said peak detector.

16.           A spread-spectrum demodulator comprising:

2                N (N is an integer not less than 2)

3   sample/hold circuits each of which samples/holds a

4   received spread signal;

5                a sample/hold control circuit which receives a

6   first clock having the same frequency as that of a clock

7   used to spread the baseband signal, and performs control

8   to make said N sample/hold circuits sequentially perform

9   sample/hold operation in synchronism with the first

10   clock;

11               a first spreading code generating circuit

12   which generates N first spreading codes in synchronism

13   with a second clock;

14               a second spreading code generating circuit

15   which generates N second spreading codes obtained by

16   rearranging the first spreading codes in reverse order

17   in synchronism with the second clock;

18               a polarity conversion circuit which outputs

19   nearly half of sample/hold output signals from said N

20   sample/hold circuits which correspond to either newer or

21   older spread signals in a reception order upon

22   performing polarity conversion such that each of the

23   sample/hold output signals exhibits two polarity states,

24   i.e., inverted and noninverted states, during one period

25   of the second clock, and outputs remaining nearly half

26   of the sample/hold signals without any change,

27                   N multipliers which multiply signals output  
28   from said polarity conversion circuit and spreading  
29   codes output from said first spreading code generating  
30   circuit or said second spreading code generating  
31   circuit;  
32                   an adder which adds outputs from said N  
33   multipliers;  
34                   a peak detector which detects a peak of an  
35   output from said adder and demodulates a data signal on  
36   the basis of the detected peak; and  
37                   a spreading code control circuit which  
38   alternately switches inputting of the first spreading  
39   codes from said first spreading code generating circuit  
40   to said multipliers and inputting of the second  
41   spreading codes from said second spreading code  
42   generating circuit to said multipliers every time the  
43   peak is detected by said peak detector.

17.               A demodulator according to claim 16, wherein  
2                   said first spreading code generating circuit  
3   comprises N flip-flop circuits of a first flip-flop  
4   circuit group each of which shifts the first spreading  
5   code in synchronism with the second clock, a first  
6   exclusive-OR circuit which receives outputs from a  
7   plurality of flip-flop circuits of said first flip-flop  
8   circuit group, and a first switch group which openably  
9   cascades the flip-flop circuits of said first flip-flop



10 circuit group and openably connects an output of said  
11 first exclusive-OR circuit to an input of a first-stage  
12 flip-flop circuit in said first flip-flop circuit group,  
13 said second spreading code generating circuit  
14 comprises N flip-flop circuits of a second flip-flop  
15 circuit group each of which shifts the second spreading  
16 code in a reverse direction relative to the first  
17 spreading code in synchronism with the second clock, a  
18 second exclusive-OR circuit which receives outputs from  
19 a plurality of flip-flop circuits in said second  
20 flip-flop circuit group, and a second switch group which  
21 openably cascades the flip-flop circuits of said second  
22 flip-flop circuit group and openably connects an output  
23 of said second exclusive-OR circuit to an input of a  
24 first-stage flip-flop circuit in said second flip-flop  
25 circuit group, and  
26 said spreading code control circuit which  
27 alternately switches control operation of turning on  
28 said first switch group and control operation of turning  
29 on said second switch group every time the peak is  
30 detected by said peak detector.

18. A spread-spectrum demodulator comprising:

2 N (N is an integer not less than 2)  
3 sample/hold circuits each of which samples/holds a  
4 received spread signal in synchronism with a first clock  
5 having the same frequency as that of a clock used to

6 spread the baseband signal;  
7                   a spreading code generating circuit which  
8 generates N spreading codes in synchronism with a second  
9 clock;  
10                   a polarity conversion circuit which outputs  
11 nearly half of the N spreading codes output from said  
12 spreading code generating circuit which correspond to  
13 either newer or older spread signals in a reception  
14 order upon performing polarity conversion such that each  
15 of the spreading codes exhibits two polarity states,  
16 i.e., inverted and noninverted states, during one period  
17 of the second clock, and outputs remaining nearly half  
18 of the codes without any change;  
19                   N multipliers which multiply signals output  
20 from said sample/hold circuits and spreading codes  
21 output from said polarity conversion circuit for each  
22 corresponding signal;  
23                   an adder which adds outputs from said N  
24 multipliers;  
25                   a peak detector which detects a peak of an  
26 output from said adder and demodulates a data signal on  
27 the basis of the detected peak; and  
28                   a clock control circuit which controls  
29 inputting of the second clock to said spreading code  
30 generating circuit in accordance with detection of the  
31 peak by said peak detector.

19.           A demodulator according to claim 18, wherein  
2   said clock control circuit alternately switches stoppage  
3   and resumption of inputting of the second clock to said  
4   spreading code generating circuit every time the peak is  
5   detected by said peak detector.

20.           A demodulator according to claim 19, wherein  
2   said clock control circuit stops inputting the second  
3   clock to said spreading code generating circuit for a  
4   predetermined period of time when the peak is detected  
5   by said peak detector.

21.           A spread-spectrum demodulator comprising:  
2                N (N is an integer not less than 2)  
3   sample/hold circuits each of which samples/holds a  
4   received spread signal in synchronism with a first clock  
5   having the same frequency as that of a clock used to  
6   spread the baseband signal;  
7                a spreading code generating circuit which  
8   generates N spreading codes in synchronism with a second  
9   clock;  
10               N multipliers which multiply signals output  
11   from said sample/hold circuits and spreading codes  
12   output from said spreading code generating circuit for  
13   each corresponding signal;  
14               a polarity conversion circuit which outputs  
15   nearly half of the multiplier output signals from said N

16 multipliers which correspond to either newer or older  
17 spread signals in a reception order upon performing  
18 polarity conversion such that each of the multiplier  
19 output signals exhibits two polarity states, i.e.,  
20 inverted and noninverted states, during one period of  
21 the second clock, and outputs remaining nearly half of  
22 the multiplier output signals without any change;  
23           an adder which adds outputs from said polarity  
24 conversion circuit;  
25           a peak detector which detects a peak of an  
26 output from said adder and demodulates a data signal on  
27 the basis of the detected peak; and  
28           a clock control circuit which controls  
29 inputting of the second clock to said spreading code  
30 generating circuit in accordance with detection of the  
31 peak by said peak detector.

22.           A demodulator according to claim 21, wherein  
2 said clock control circuit alternately switches stoppage  
3 and resumption of inputting of the second clock to said  
4 spreading code generating circuit every time the peak is  
5 detected by said peak detector.

23.           A demodulator according to claim 21, wherein  
2 said clock control circuit stops inputting the second  
3 clock to said spreading code generating circuit for a  
4 predetermined period of time when the peak is detected

5 by said peak detector.

24. A spread-spectrum demodulator comprising:

2 N (N is an integer not less than 2)

3 sample/hold circuits each of which samples/holds a  
4 received spread signal in synchronism with a first clock  
5 having the same frequency as that of a clock used to  
6 spread the baseband signal;

7 a spreading code generating circuit which  
8 generates N spreading codes in synchronism with a second  
9 clock;

10 a polarity conversion circuit which outputs  
11 nearly half of the sample/hold output signals from said  
12 N sample/hold circuits which correspond to either newer  
13 or older spread signals in a reception order upon  
14 performing polarity conversion such that each of the  
15 sample/hold output signals exhibits two polarity states,  
16 i.e., inverted and noninverted states, during one period  
17 of the second clock, and outputs remaining nearly half  
18 of the sample/hold output signals without any change;

19 N multipliers which multiply signals output  
20 from said polarity conversion circuit and spreading  
21 codes output from said spreading code generating circuit  
22 for each corresponding signal;

23 an adder which adds outputs from said N  
24 multipliers;

25 a peak detector which detects a peak of an

26 output from said adder and demodulates a data signal on  
27 the basis of the detected peak; and  
28 a clock control circuit which controls  
29 inputting of the second clock to said spreading code  
30 generating circuit in accordance with detection of the  
31 peak by said peak detector.

25. A demodulator according to claim 24, wherein  
2 said clock control circuit alternately switches stoppage  
3 and resumption of inputting of the second clock to said  
4 spreading code generating circuit every time the peak is  
5 detected by said peak detector.

26. A demodulator according to claim 24, wherein  
2 said clock control circuit stops inputting the second  
3 clock to said spreading code generating circuit for a  
4 predetermined period of time when the peak is detected  
5 by said peak detector.

27. A spread-spectrum demodulator comprising:  
2 a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;  
6  $(N - 1)$  ( $N$  is an integer not less than 2)  
7 register circuits which output  $(N - 1)$  signals by  
8 delaying an output signal from said comparator circuit

9 by one period to  $(N - 1)$  periods of the first clock,  
10 respectively;

11 a first spreading code generating circuit  
12 which generates  $N$  first spreading codes in synchronism  
13 with a second clock;

14 a second spreading code generating circuit  
15 which generates  $N$  second spreading codes obtained by  
16 rearranging the first spreading codes in reverse order  
17 in synchronism with the second clock;

18 a polarity conversion circuit which outputs  
19 nearly half of the  $N$  spreading codes output from said  
20 first spreading code generating circuit or said second  
21 spreading code generating circuit which correspond to  
22 either newer or older spread signals in a reception  
23 order upon performing polarity conversion such that each  
24 of the spreading codes exhibits two polarity states,  
25 i.e., inverted and noninverted states, during one period  
26 of the second clock, and outputs remaining nearly half  
27 of the codes without any change,

28  $N$  multipliers which multiply signals output  
29 from said comparator circuit and said register circuits  
30 and spreading codes output from said spreading code  
31 generating circuit for each corresponding signal;

32 an adder which adds outputs from said  $N$   
33 multipliers;

34 a peak detector which detects a peak of an  
35 output from said adder and demodulates a data signal on

36 the basis of the detected peak; and  
37 a spreading code control circuit which  
38 alternately switches inputting of the first spreading  
39 codes from said first spreading code generating circuit  
40 to said polarity conversion circuit and inputting of the  
41 second spreading codes from said second spreading code  
42 generating circuit to said polarity conversion circuit  
43 every time the peak is detected by said peak detector.

28. A demodulator according to claim 27, wherein  
2 said register circuit comprises a flip-flop  
3 circuit,  
4 said first spreading code generating circuit  
5 comprises N flip-flop circuits of a first flip-flop  
6 circuit group each of which shifts the first spreading  
7 code in synchronism with the second clock, a first  
8 exclusive-OR circuit which receives outputs from a  
9 plurality of flip-flop circuits of said first flip-flop  
10 circuit group, and a first switch group which openably  
11 cascades the flip-flop circuits of said first flip-flop  
12 circuit group and openably connects an output of said  
13 first exclusive-OR circuit to an input of a first-stage  
14 flip-flop circuit in said first flip-flop circuit group,  
15 said second spreading code generating circuit  
16 comprises N flip-flop circuits of a second flip-flop  
17 circuit group each of which shifts the second spreading  
18 code in a reverse direction relative to the first



19 spreading code in synchronism with the second clock, a  
20 second exclusive-OR circuit which receives outputs from  
21 a plurality of flip-flop circuits in said second  
22 flip-flop circuit group, and a second switch group which  
23 openably cascades the flip-flop circuits of said second  
24 flip-flop circuit group and openably connects an output  
25 of said second exclusive-OR circuit to an input of a  
26 first-stage flip-flop circuit in said second flip-flop  
27 circuit group, and  
28               said spreading code control circuit which  
29 alternately switches control operation of turning on  
30 said first switch group and control operation of turning  
31 on said second switch group every time the peak is  
32 detected by said peak detector.

29.           A spread-spectrum demodulator comprising:  
2               a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;  
6                $(N - 1)$  ( $N$  is an integer not less than 2)  
7 register circuits which output  $(N - 1)$  signals by  
8 delaying an output signal from said comparator circuit  
9 by one period to  $(N - 1)$  periods of the first clock,  
10 respectively;  
11               a first spreading code generating circuit  
12 which generates  $N$  first spreading codes in synchronism

13 with a second clock;  
14               a second spreading code generating circuit  
15 which generates N second spreading codes obtained by  
16 rearranging the first spreading codes in reverse order  
17 in synchronism with the second clock;  
18               N multipliers which multiply signals output  
19 from said comparator circuit and said register circuits  
20 and spreading codes output from said first spreading  
21 code generating circuit or said second spreading  
22 generating circuit for each corresponding signal;  
23               a polarity conversion circuit which outputs  
24 nearly half of the multiplier output signals from said N  
25 multipliers which correspond to either newer or older  
26 spread signals in a reception order upon performing  
27 polarity conversion such that each of the multiplier  
28 output signals exhibits two polarity states, i.e.,  
29 inverted and noninverted states, during one period of  
30 the second clock, and outputs remaining nearly half of  
31 the multiplier output signals without any change,  
32               an adder which adds outputs from said polarity  
33 conversion circuit;  
34               a peak detector which detects a peak of an  
35 output from said adder and demodulates a data signal on  
36 the basis of the detected peak; and  
37               a spreading code control circuit which  
38 alternately switches inputting of the first spreading  
39 codes from said first spreading code generating circuit

40 to said multipliers and inputting of the second  
41 spreading codes from said second spreading code  
42 generating circuit to said multipliers time the peak is  
43 detected by said peak detector.

30. A demodulator according to claim 29, wherein  
2 said register circuit comprises a flip-flop  
3 circuit,  
4 said first spreading code generating circuit  
5 comprises N flip-flop circuits of a first flip-flop  
6 circuit group each of which shifts the first spreading  
7 code in synchronism with the second clock, a first  
8 exclusive-OR circuit which receives outputs from a  
9 plurality of flip-flop circuits of said first flip-flop  
10 circuit group, and a first switch group which openably  
11 cascades the flip-flop circuits of said first flip-flop  
12 circuit group and openably connects an output of said  
13 first exclusive-OR circuit to an input of a first-stage  
14 flip-flop circuit in said first flip-flop circuit group,  
15 said second spreading code generating circuit  
16 comprises N flip-flop circuits of a second flip-flop  
17 circuit group each of which shifts the second spreading  
18 code in a reverse direction relative to the first  
19 spreading code in synchronism with the second clock, a  
20 second exclusive-OR circuit which receives outputs from  
21 a plurality of flip-flop circuits in said second  
22 flip-flop circuit group, and a second switch group which

23 openably cascades the flip-flop circuits of said second  
24 flip-flop circuit group and openably connects an output  
25 of said second exclusive-OR circuit to an input of a  
26 first-stage flip-flop circuit in said second flip-flop  
27 circuit group, and  
28               said spreading code control circuit which  
29 alternately switches control operation of turning on  
30 said first switch group and control operation of turning  
31 on said second switch group every time the peak is  
32 detected by said peak detector.

31.           A spread-spectrum demodulator comprising:  
2               a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;  
6                $(N - 1)$  ( $N$  is an integer not less than 2)  
7 register circuits which output  $(N - 1)$  signals by  
8 delaying an output signal from said comparator circuit  
9 by one period to  $(N - 1)$  periods of the first clock,  
10 respectively;  
11               a first spreading code generating circuit  
12 which generates  $N$  first spreading codes in synchronism  
13 with a second clock;  
14               a second spreading code generating circuit  
15 which generates  $N$  second spreading codes obtained by  
16 rearranging the first spreading codes in reverse order

17 in synchronism with the second clock;  
18           a polarity conversion circuit which outputs  
19 nearly half of output signals from said comparator  
20 circuit and said register circuits which correspond to  
21 either newer or older spread signals in a reception  
22 order upon performing polarity conversion such that each  
23 of the output signals exhibits two polarity states,  
24 i.e., inverted and noninverted states, during one period  
25 of the second clock, and outputs remaining nearly half  
26 of the output signals without any change,  
27           N multipliers which multiply signals output  
28 from said polarity conversion circuit and spreading  
29 codes output from said first spreading code generating  
30 circuit or said second spreading generating circuit for  
31 each corresponding signal;  
32           an adder which adds outputs from said N  
33 multipliers;  
34           a peak detector which detects a peak of an  
35 output from said adder and demodulates a data signal on  
36 the basis of the detected peak; and  
37           a spreading code control circuit which  
38 alternately switches inputting of the first spreading  
39 codes from said first spreading code generating circuit  
40 to said multipliers and inputting of the second  
41 spreading codes from said second spreading code  
42 generating circuit to said multipliers time the peak is  
43 detected by said peak detector.

32.           A demodulator according to claim 31, wherein  
2               said register circuit comprises a flip-flop  
3 circuit,  
4               said first spreading code generating circuit  
5 comprises N flip-flop circuits of a first flip-flop  
6 circuit group each of which shifts the first spreading  
7 code in synchronism with the second clock, a first  
8 exclusive-OR circuit which receives outputs from a  
9 plurality of flip-flop circuits of said first flip-flop  
10 circuit group, and a first switch group which openably  
11 cascades the flip-flop circuits of said first flip-flop  
12 circuit group and openably connects an output of said  
13 first exclusive-OR circuit to an input of a first-stage  
14 flip-flop circuit in said first flip-flop circuit group,  
15               said second spreading code generating circuit  
16 comprises N flip-flop circuits of a second flip-flop  
17 circuit group each of which shifts the second spreading  
18 code in a reverse direction relative to the first  
19 spreading code in synchronism with the second clock, a  
20 second exclusive-OR circuit which receives outputs from  
21 a plurality of flip-flop circuits in said second  
22 flip-flop circuit group, and a second switch group which  
23 openably cascades the flip-flop circuits of said second  
24 flip-flop circuit group and openably connects an output  
25 of said second exclusive-OR circuit to an input of a  
26 first-stage flip-flop circuit in said second flip-flop

27 circuit group, and  
28               said spreading code control circuit which  
29 alternately switches control operation of turning on  
30 said first switch group and control operation of turning  
31 on said second switch group every time the peak is  
32 detected by said peak detector.

33.           A spread-spectrum demodulator comprising:  
2               a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;  
6                $(N - 1)$  ( $N$  is an integer not less than 2)  
7 register circuits which output  $(N - 1)$  signals by  
8 delaying an output signal from said comparator circuit  
9 by one period to  $(N - 1)$  periods of the first clock,  
10 respectively;  
11               a spreading code generating circuit which  
12 generates  $N$  spreading codes in synchronism with a second  
13 clock;  
14               a polarity conversion circuit which outputs  
15 nearly half of  $N$  spreading codes output from said  
16 spreading code generating circuit which correspond to  
17 either newer or older spread signals in a reception  
18 order upon performing polarity conversion such that each  
19 of the spreading codes exhibits two polarity states,  
20 i.e., inverted and noninverted states, during one period

21 of the second clock, and outputs remaining nearly half  
22 of the codes without any change,  
23 N multipliers which multiply signals output  
24 from said comparator circuit and said register circuits  
25 and spreading codes output from said polarity conversion  
26 circuit for each corresponding signal;  
27 an adder which adds outputs from said N  
28 multipliers;  
29 a peak detector which detects a peak of an  
30 output from said adder and demodulates a data signal on  
31 the basis of the detected peak; and  
32 a clock control circuit which controls  
33 inputting of the second clock to said spreading code  
34 generating circuit in accordance with detection of the  
35 peak by said peak detector.

34. A demodulator according to claim 33, wherein  
2 said clock control circuit alternately switches stoppage  
3 and resumption of inputting of the second clock to said  
4 spreading code generating circuit every time the peak is  
5 detected by said peak detector.

35. A demodulator according to claim 33, wherein  
2 said clock control circuit stops inputting the second  
3 clock to said spreading code generating circuit for a  
4 predetermined period of time when the peak is detected  
5 by said peak detector.



36.           A spread-spectrum demodulator comprising:

2               a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;

6               (N - 1) (N is an integer not less than 2)  
7 register circuits which output (N - 1) signals by  
8 delaying an output signal from said comparator circuit  
9 by one period to (N - 1) periods of the first clock,  
10 respectively;

11              a spreading code generating circuit which  
12 generates N spreading codes in synchronism with a second  
13 clock;

14              N multipliers which multiply signals output  
15 from said comparator circuit and said register circuits  
16 and spreading codes output from said spreading code  
17 generating circuit for each corresponding signal;

18              a polarity conversion circuit which outputs  
19 nearly half of multiplier output signals from said N  
20 multipliers which correspond to either newer or older  
21 spread signals in a reception order upon performing  
22 polarity conversion such that each of the multiplier  
23 output signals exhibits two polarity states, i.e.,  
24 inverted and noninverted states, during one period of  
25 the second clock, and outputs remaining nearly half of  
26 the multiplier output signals without any change,

27                   an adder which adds outputs from said polarity  
28 conversion circuit;  
29                   a peak detector which detects a peak of an  
30 output from said adder and demodulates a data signal on  
31 the basis of the detected peak; and  
32                   a clock control circuit which controls  
33 inputting of the second clock to said spreading code  
34 generating circuit in accordance with detection of the  
35 peak by said peak detector.

37.           A demodulator according to claim 36, wherein  
2 said clock control circuit alternately switches stoppage  
3 and resumption of inputting of the second clock to said  
4 spreading code generating circuit every time the peak is  
5 detected by said peak detector.

38.           A demodulator according to claim 36, wherein  
2 said clock control circuit stops inputting the second  
3 clock to said spreading code generating circuit for a  
4 predetermined period of time when the peak is detected  
5 by said peak detector.

39.           A spread-spectrum demodulator comprising:  
2                   a comparator which converts a received spread  
3 signal into a digital signal in synchronism with a first  
4 clock having the same frequency as that of a clock used  
5 to spread the baseband signal;

6                   (N - 1) (N is an integer not less than 2)  
7   register circuits which output (N - 1) signals by  
8   delaying an output signal from said comparator circuit  
9   by one period to (N - 1) periods of the first clock,  
10   respectively;  
11                   a spreading code generating circuit which  
12   generates N spreading codes in synchronism with a second  
13   clock;  
14                   a polarity conversion circuit which outputs  
15   nearly half of output signals from said comparator  
16   circuit and said sample/hold circuits which correspond  
17   to either newer or older spread signals in a reception  
18   order upon performing polarity conversion such that each  
19   of the output signals exhibits two polarity states,  
20   i.e., inverted and noninverted states, during one period  
21   of the second clock, and outputs remaining nearly half  
22   of the output signals without any change,  
23                   N multipliers which multiply signals output  
24   from said polarity conversion circuit and spreading  
25   codes output from said spreading code generating circuit  
26   for each corresponding signal;  
27                   an adder which adds outputs from said N  
28   multipliers;  
29                   a peak detector which detects a peak of an  
30   output from said adder and demodulates a data signal on  
31   the basis of the detected peak; and  
32                   a clock control circuit which controls

33 inputting of the second clock to said spreading code  
34 generating circuit in accordance with detection of the  
35 peak by said peak detector.

40. A demodulator according to claim 39, wherein  
2 said clock control circuit alternately switches stoppage  
3 and resumption of inputting of the second clock to said  
4 spreading code generating circuit every time the peak is  
5 detected by said peak detector.

41. A demodulator according to claim 39, wherein  
2 said clock control circuit stops inputting the second  
3 clock to said spreading code generating circuit for a  
4 predetermined period of time when the peak is detected  
5 by said peak detector.

42. A demodulator according to claim 3, wherein  
2 inputs of the respective flip-flop circuits of said  
3 first flip-flop circuit group excluding the first-stage  
4 flip-flop circuit, are connected to inputs of the  
5 respective flip-flop circuits of said second flip-flop  
6 circuit group excluding the first-stage flip-flop  
7 circuit, for each corresponding circuit, to output the  
8 first spreading codes or second spreading codes from the  
9 respective flip-flop circuits of said first flip-flop  
10 circuit group.

43.           A demodulator according to claim 42, wherein  
2               said peak detector comprises means for  
3 determining a reference level from a peak level of an  
4 output from said adder and a predetermined lower limit  
5 level, and means for comparing the reference level with  
6 an output from said adder to generate a control signal  
7 synchronized with a trailing edge of a peak signal of an  
8 output from said adder, and  
9               said spreading code control circuit  
10 alternately switches control operation of turning on  
11 said first switch group and control operation of turning  
12 on said second switch group every time the control  
13 signal is output.

44.           A demodulator according to claim 42, wherein  
2               said peak detector comprises means for determining the  
3 lower limit level on the basis of a power supply voltage  
4 and a common mode level.

45.           A demodulator according to claim 11, wherein  
2               inputs of the respective flip-flop circuits of said  
3 first flip-flop circuit group excluding the first-stage  
4 flip-flop circuit, are connected to inputs of the  
5 respective flip-flop circuits of said second flip-flop  
6 circuit group excluding the first-stage flip-flop  
7 circuit, for each corresponding circuit, to output the  
8 first spreading codes or second spreading codes from the

9    respective flip-flop circuits of said first flip-flop  
10   circuit group.

46.       A demodulator according to claim 45, wherein  
2           said peak detector comprises means for  
3   determining a reference level from a peak level of an  
4   output from said adder and a predetermined lower limit  
5   level, and means for comparing the reference level with  
6   an output from said adder to generate a control signal  
7   synchronized with a trailing edge of a peak signal of an  
8   output from said adder, and  
9           said spreading code control circuit  
10   alternately switches control operation of turning on  
11   said first switch group and control operation of turning  
12   on said second switch group every time the control  
13   signal is output.

47.       A demodulator according to claim 45, wherein  
2   said peak detector comprises means for determining the  
3   lower limit level on the basis of a power supply voltage  
4   and a common mode level.

48.       A demodulator according to claim 13, wherein  
2   inputs of the respective flip-flop circuits of said  
3   first flip-flop circuit group excluding the first-stage  
4   flip-flop circuit, are connected to inputs of the  
5   respective flip-flop circuits of said second flip-flop

6 circuit group excluding the first-stage flip-flop  
7 circuit, for each corresponding circuit, to output the  
8 first spreading codes or second spreading codes from the  
9 respective flip-flop circuits of said first flip-flop  
10 circuit group.

49. A demodulator according to claim 48, wherein  
2 said peak detector comprises means for  
3 determining a reference level from a peak level of an  
4 output from said adder and a predetermined lower limit  
5 level, and means for comparing the reference level with  
6 an output from said adder to generate a control signal  
7 synchronized with a trailing edge of a peak signal of an  
8 output from said adder, and  
9 said spreading code control circuit  
10 alternately switches control operation of turning on  
11 said first switch group and control operation of turning  
12 on said second switch group every time the control  
13 signal is output.

50. A demodulator according to claim 48, wherein  
2 said peak detector comprises means for determining the  
3 lower limit level on the basis of a power supply voltage  
4 and a common mode level.

51. A demodulator according to claim 15, wherein  
2 inputs of the respective flip-flop circuits of said

3 first flip-flop circuit group excluding the first-stage  
4 flip-flop circuit, are connected to inputs of the  
5 respective flip-flop circuits of said second flip-flop  
6 circuit group excluding the first-stage flip-flop  
7 circuit, for each corresponding circuit, to output the  
8 first spreading codes or second spreading codes from the  
9 respective flip-flop circuits of said first flip-flop  
10 circuit group.

52. A demodulator according to claim 51, wherein  
2 said peak detector comprises means for  
3 determining a reference level from a peak level of an  
4 output from said adder and a predetermined lower limit  
5 level, and means for comparing the reference level with  
6 an output from said adder to generate a control signal  
7 synchronized with a trailing edge of a peak signal of an  
8 output from said adder, and  
9 said spreading code control circuit  
10 alternately switches control operation of turning on  
11 said first switch group and control operation of turning  
12 on said second switch group every time the control  
13 signal is output.

53. A demodulator according to claim 51, wherein  
2 said peak detector comprises means for determining the  
3 lower limit level on the basis of a power supply voltage  
4 and a common mode level.



54.           A demodulator according to claim 17, wherein  
2   inputs of the respective flip-flop circuits of said  
3   first flip-flop circuit group excluding the first-stage  
4   flip-flop circuit, are connected to inputs of the  
5   respective flip-flop circuits of said second flip-flop  
6   circuit group excluding the first-stage flip-flop  
7   circuit, for each corresponding circuit, to output the  
8   first spreading codes or second spreading codes from the  
9   respective flip-flop circuits of said first flip-flop  
10  circuit group.

55.           A demodulator according to claim 54, wherein  
2               said peak detector comprises means for  
3   determining a reference level from a peak level of an  
4   output from said adder and a predetermined lower limit  
5   level, and means for comparing the reference level with  
6   an output from said adder to generate a control signal  
7   synchronized with a trailing edge of a peak signal of an  
8   output from said adder, and  
9               said spreading code control circuit  
10  alternately switches control operation of turning on  
11  said first switch group and control operation of turning  
12  on said second switch group every time the control  
13  signal is output.

56.           A demodulator according to claim 54, wherein

2 said peak detector comprises means for determining the  
3 lower limit level on the basis of a power supply voltage  
4 and a common mode level.

57. A demodulator according to claim 28, wherein  
2 inputs of the respective flip-flop circuits of said  
3 first flip-flop circuit group excluding the first-stage  
4 flip-flop circuit, are connected to inputs of the  
5 respective flip-flop circuits of said second flip-flop  
6 circuit group excluding the first-stage flip-flop  
7 circuit, for each corresponding circuit, to output the  
8 first spreading codes or second spreading codes from the  
9 respective flip-flop circuits of said first flip-flop  
10 circuit group.

58. A demodulator according to claim 57, wherein  
2 said peak detector comprises means for  
3 determining a reference level from a peak level of an  
4 output from said adder and a predetermined lower limit  
5 level, and means for comparing the reference level with  
6 an output from said adder to generate a control signal  
7 synchronized with a trailing edge of a peak signal of an  
8 output from said adder, and  
9 said spreading code control circuit  
10 alternately switches control operation of turning on  
11 said first switch group and control operation of turning  
12 on said second switch group every time the control

13 signal is output.

59. A demodulator according to claim 57, wherein  
2 said peak detector comprises means for determining the  
3 lower limit level on the basis of a power supply voltage  
4 and a common mode level.

60. A demodulator according to claim 30, wherein  
2 inputs of the respective flip-flop circuits of said  
3 first flip-flop circuit group excluding the first-stage  
4 flip-flop circuit, are connected to inputs of the  
5 respective flip-flop circuits of said second flip-flop  
6 circuit group excluding the first-stage flip-flop  
7 circuit, for each corresponding circuit, to output the  
8 first spreading codes or second spreading codes from the  
9 respective flip-flop circuits of said first flip-flop  
10 circuit group.

61. A demodulator according to claim 60, wherein  
2 said peak detector comprises means for  
3 determining a reference level from a peak level of an  
4 output from said adder and a predetermined lower limit  
5 level, and means for comparing the reference level with  
6 an output from said adder to generate a control signal  
7 synchronized with a trailing edge of a peak signal of an  
8 output from said adder, and  
9 said spreading code control circuit

10 alternately switches control operation of turning on  
11 said first switch group and control operation of turning  
12 on said second switch group every time the control  
13 signal is output.

62. A demodulator according to claim 60, wherein  
2 said peak detector comprises means for determining the  
3 lower limit level on the basis of a power supply voltage  
4 and a common mode level.

63. A demodulator according to claim 32, wherein  
2 inputs of the respective flip-flop circuits of said  
3 first flip-flop circuit group excluding the first-stage  
4 flip-flop circuit, are connected to inputs of the  
5 respective flip-flop circuits of said second flip-flop  
6 circuit group excluding the first-stage flip-flop  
7 circuit, for each corresponding circuit, to output the  
8 first spreading codes or second spreading codes from the  
9 respective flip-flop circuits of said first flip-flop  
10 circuit group.

64. A demodulator according to claim 63, wherein  
2 said peak detector comprises means for  
3 determining a reference level from a peak level of an  
4 output from said adder and a predetermined lower limit  
5 level, and means for comparing the reference level with  
6 an output from said adder to generate a control signal

7     synchronized with a trailing edge of a peak signal of an  
8     output from said adder, and  
9             said spreading code control circuit  
10    alternately switches control operation of turning on  
11    said first switch group and control operation of turning  
12    on said second switch group every time the control  
13    signal is output.

65.         A demodulator according to claim 63, wherein  
2    said peak detector comprises means for determining the  
3    lower limit level on the basis of a power supply voltage  
4    and a common mode level.

66.         A demodulator according to claim 1, further  
2    comprising a filter which passes only a signal  
3    component, of a signal output from said data signal  
4    demodulating section, which falls within a data  
5    frequency band.

67.         A demodulator according to claim 1, further  
2    comprising demodulation means for demodulating a data  
3    signal by counting peaks of outputs from said  
4    correlation value computing section in place of said  
5    data signal demodulating section.